REMARKS

Claims 3-12 and 13-30, as amended, remain in this application. Claims 1, 2, and 13 have been cancelled. In view of the foregoing amendments, and remarks that follow, Applicant respectfully requests reconsideration and timely indication of allowance.

1. *Claims 14-28.*

The Examiner has indicated that claim 14 is directed to patentable subject matter. The Examiner has objected to claim 14, however, as being dependent on a rejected base claim indicating that allowance would be forthcoming if claim 14 was rewritten in independent form. Although Applicant does not necessarily agree with the rejection of the base claim, to advance the prosecution of this case, claim 14 has be amended accordingly. Applicant respectfully submits that claim 14 is now ready for allowance.

Claims 15-28 are dependent from claim 14, and therefore, include all the limitations therein. Accordingly, these claims are also allowable.

2. *Claims1-13 and 30.*

Claims 1-4, 13 and 30 were rejected under 35 U.S.C. 102(b) as being anticipated by Chappell et al. These rejections are respectively traversed to the extent they are applicable to the claims remaining in this case.

Applicant discloses a novel and unobvious high performance, low leakage integrated circuit. The integrated circuit may be configured with first and second circuit components with their outputs tied together. When the integrated circuit enters the sleep mode, the output of the second circuit component may be fed back to the input of the first circuit component to force the first circuit component into a state wherein a leakage path from power to ground through a transistor in the first circuit component and a transistor in the second circuit component is blocked. The feedback basically ensures that when the transistor in the second circuit component is turned ON, the transistor in the first circuit component is forced into an OFF state. The data input to the first circuit component may be multiplexed with the feedback. In this way, the data may be preserved when the integrated circuit comes out of the sleep mode.

The Examiner takes the position that Chappell discloses Applicant's approach. According to the Examiner, feedback from a second FET Q2 may be applied to the input of a first FET Q3 to block a leakage path from power to ground through the two transistors. The feedback forces the first FET Q3 into the OFF state when the second FET Q2 is in the ON state. The Examiner further contends that when the data-input is in the standby state, the data is preserved by the first FET Q3, and the inverter 82 that precedes it. With respect to the latter contention, the Examiner's position is factually incorrect.

First, it is not clear whether the "standby" condition disclosed in Chappell is the same as the "sleep mode" disclosed by Applicant. But even more important, the combination of the first FET Q3 and the inverter 82 does not preserve the data in the standby state. To the contrary, FET QD3 "force[s] automatic resetting of the input-node A . . . when the data-input returns to its standby-state." (Chappell, col. 7: 60-64). More specifically, the FET QD3 is forced into the ON state in the standby mode. As a result, the input-node A is forced to ground in response to an input pulse applied to the second FET Q2. The ground at the input-node A forces the output of the inverter 82 into the high state, thus turning OFF the first FET Q3. In other words, the output of both the first FET Q3 and the inverter 82 are forced into a particular state in the standby mode, regardless of the state or data that existed prior. As a result, the data is not preserved, but rather lost.

Referring now to the specific claims, Applicant submits that they recite subject matter which is neither disclosed nor suggested by Chappell. Independent claims 3 and 30 each recite an integrated circuit that uses feedback during a sleep mode to block leakage, while at the same time "***preserving data in said integrated circuit***." (emphasis added). The circuit identified by the Examiner in Chappell, on the other hand, resets the data when in the standby mode. Accordingly, Chappell is legally insufficient to support an anticipatory rejection of claims 3 and 30.

Claims 4-12 are dependent from claim 3, and therefore, include all the limitations therein. Accordingly, these claims are also allowable for the same reasons set forth hereinbefore, as well as the additional limitations recited therein. These additional limitations will not be addressed at this time because the Examiner has not established that claim 3 is anticipated.

3. *Claim 29*.

Claim 29 has been rejected under 35 U.S.C. 112, second paragraph as allegedly being indefinite. Applicant respectfully traverses this rejection.

Claim 29 recites in part:

> means for employing feedback within said circuit to block leakage paths through said one of the LVT transistors via one or more of said HVT transistors....

The Examiner takes the position that the language "via one or more of said HVT transistors" is vague and indefinite. According to the Examiner, it is not clear what is meant by this language. In response, the Examiner is directed to FIG. 3 of the above-identified patent application where feedback from the output of the second inverter 100 is applied through the multiplexer 82 to the gates of HVT transistors T20, T22 at the input to the first inverter 96. A "low" input to the second inverter 100 turns the HVT transistor T26 OFF, and the feedback from the second inverter turns OFF the HVT transistor T22 in the first inverter 96. As a result, the leakage path from power to ground through the HVT transistor T20 in the first inverter 96 is blocked by the HVT transistor T26 in the second inverter 100, and the leakage path from power to ground through the HVT transistor T24 in the second inverter 100 is blocked by the HVT transistor T22 in the first inverter 96. Both leakage paths go through additional intervening circuitry 98, which includes an LVT transistor (see FIG. 4, LVT transistor 114).

A similar analysis may be applied to a "high" input to the second inverter 100, with the HVT transistor T20 blocking one leakage path through the LVT transistor, and the HVT transistor T24 blocking the other leakage path through the LVT transistor.

Accordingly, it is respectfully requested that this rejection be withdrawn. Since the Examiner has failed to cite any prior art against claim 29, Applicant respectfully submits that this claim is ready for allowance.

4. *Title of the Patent Application*

The title of the patent application has been objected to by the Examiner for allegedly failing to adequately describe the claimed invention. Although Applicant does not agree with the Examiner's objection, to expedite the prosecution of this application, the title has been amended accordingly. Applicant respectfully requests that this objection be withdrawn.

5. *Objection to the Disclosure.*

The Examiner has objected to the disclosure based on a number inadvertent typographical and/or clerical errors. In response to this objection, the disclosure has been amended to correct these errors. Accordingly, Applicant respectfully requests that the objection to the disclosure be withdrawn.

6. *Objection to the Drawings.*

The Examiner has further objected to the drawings based on minor drawing errors. In response, Applicant submit herewith proposed drawing corrections in accordance with MPEP § 608.02(v) along with a separate letter to the Official Draftsperson pursuant to MPEP § 608.02(r). Approval of the proposed drawing corrections is respectfully requested. Formal drawings incorporating the proposed corrections will be filed after a Notice of Allowance is received.

7. *Objection to the Claims.*

The claims have been object to based on various minor informalities. In response to this objection, the claims have been amended accordingly. Applicant respectfully requests that this objection be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested. Should any issues remain which the Examiner believes could be resolved in a telephone interview, the Examiner is requested to telephone Applicant's undersigned attorney.

If there are any fees due in connection with the filing of this response, please charge such fees to our Deposit Account No. 17-0026. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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